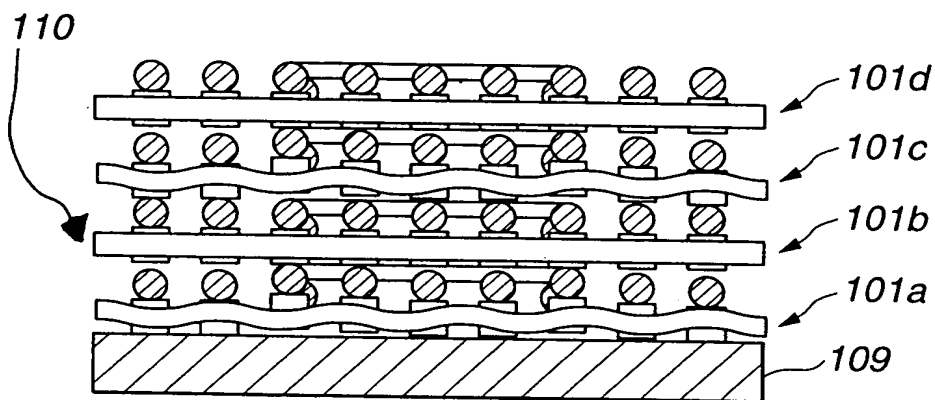
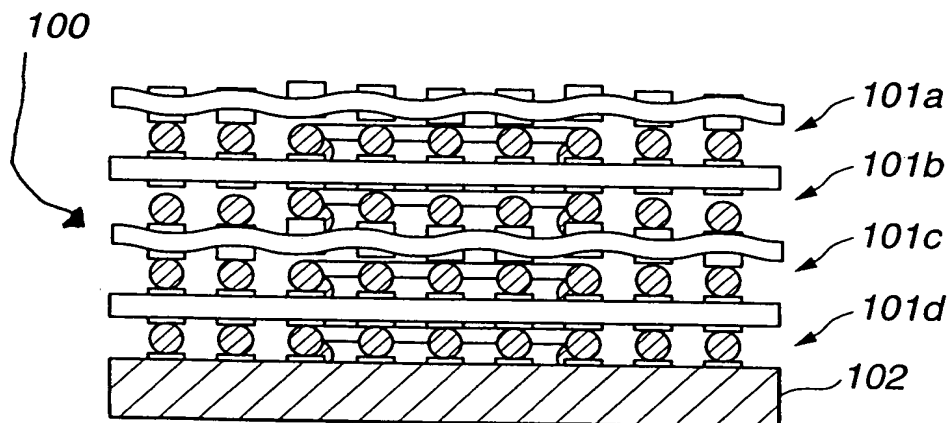


**FIG.1(a)**



**FIG.1(b)**



**FIG.1(c)**

FIG.2(a)

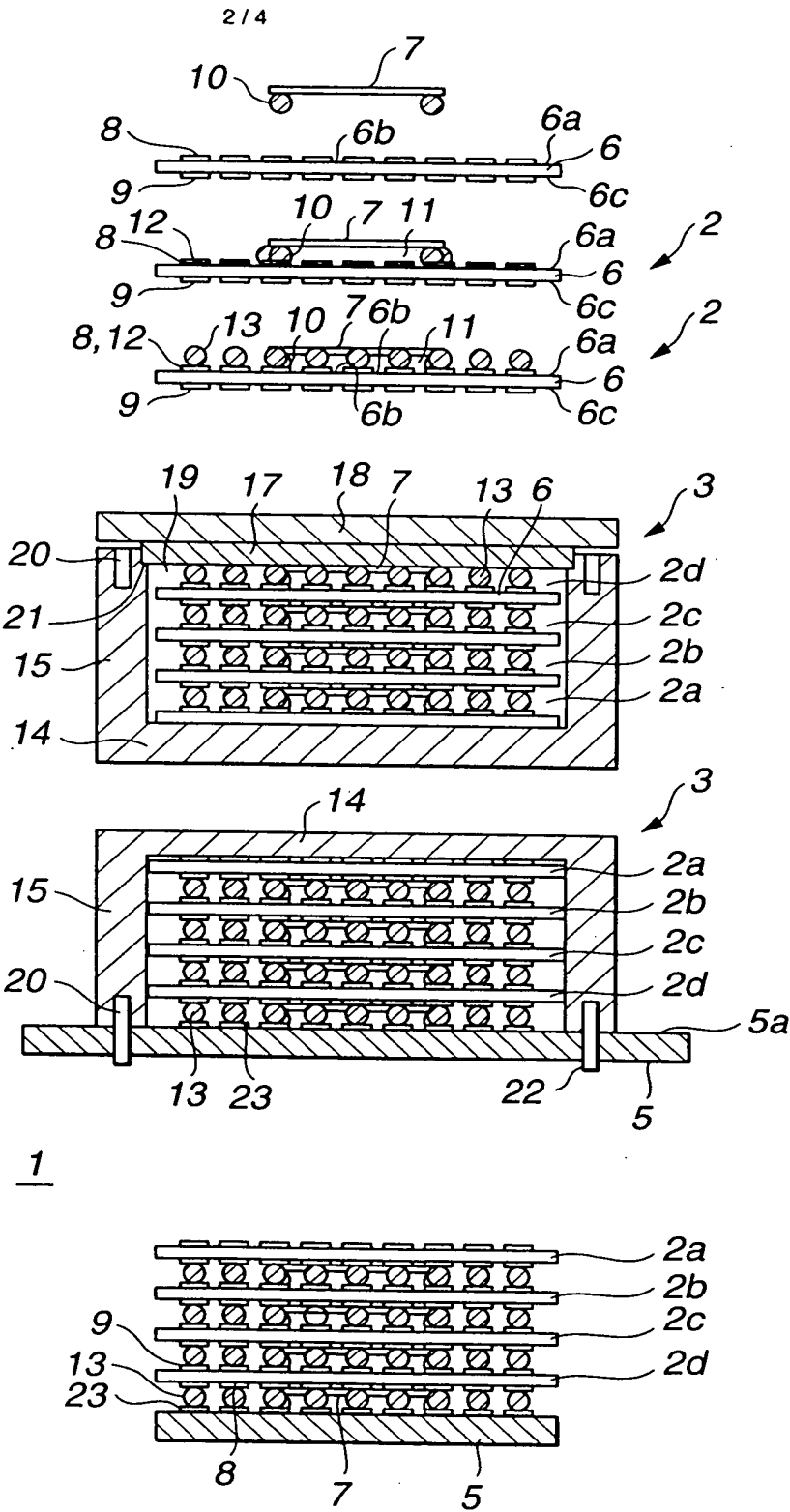
FIG.2(b)

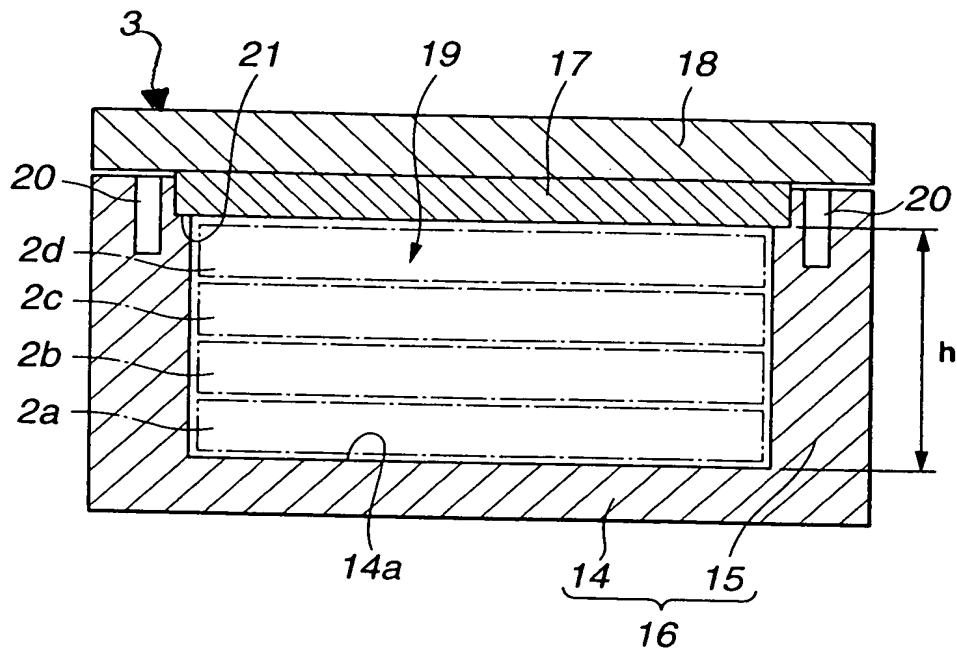
FIG.2(c)

FIG.2(d)

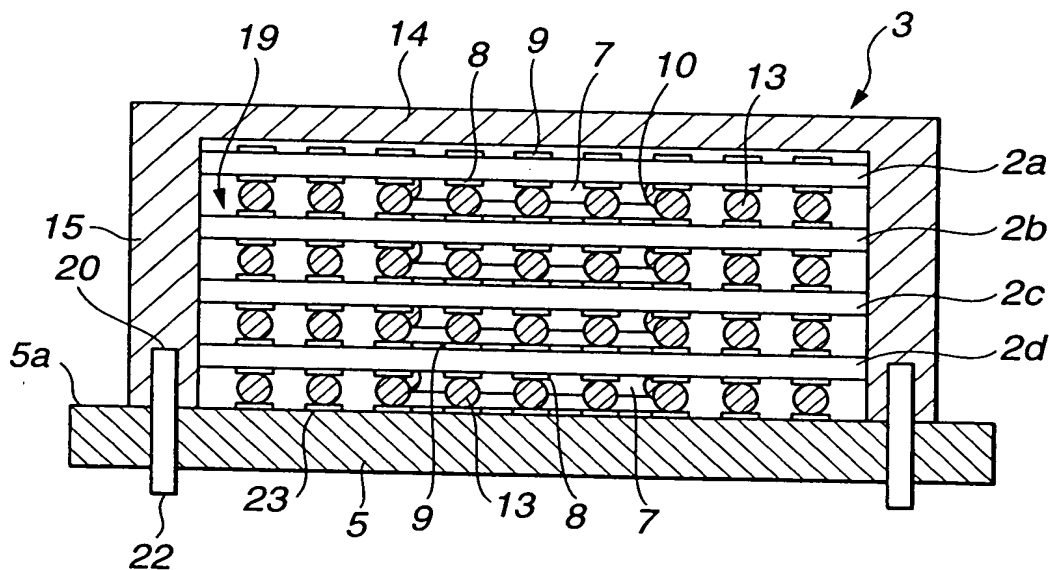
FIG.2(e)

FIG.2 (f)





**FIG. 3**



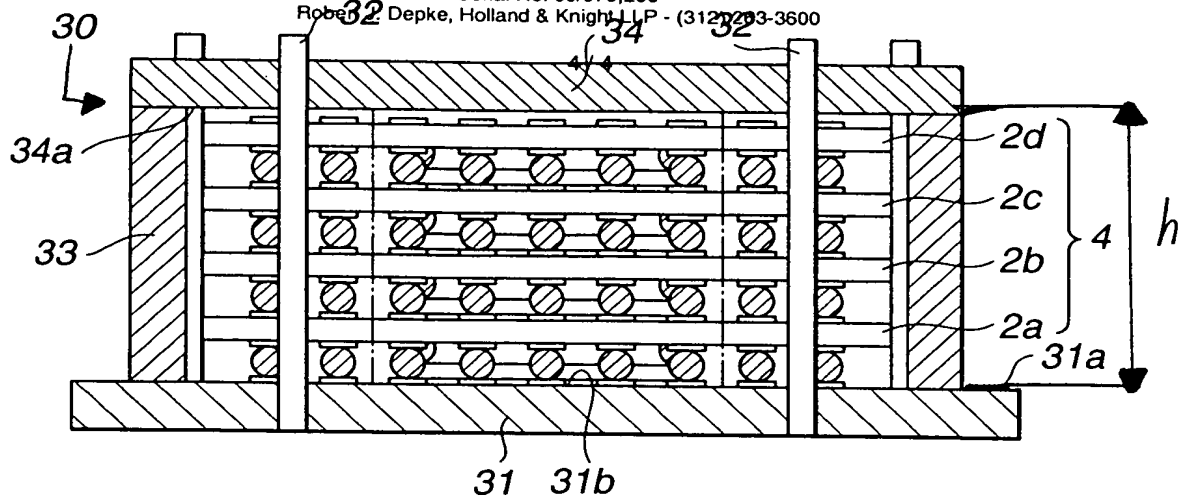
**FIG. 4**

ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE  
REPLACEMENT DRAWINGS

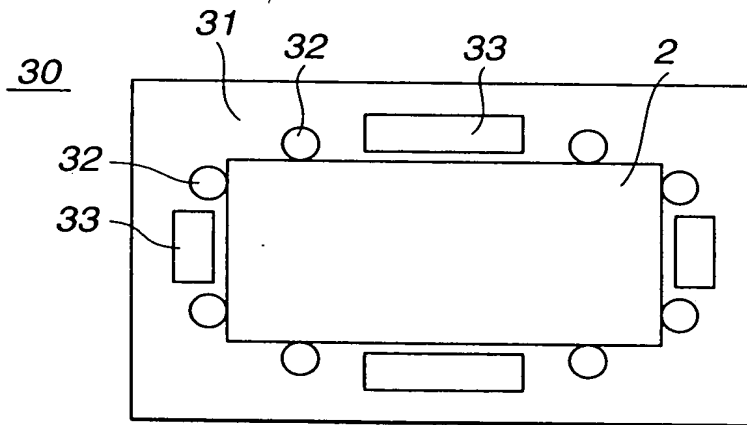
Inventor: Yoshiyuki Yanagisawa et al.

Serial No. 09/876,290

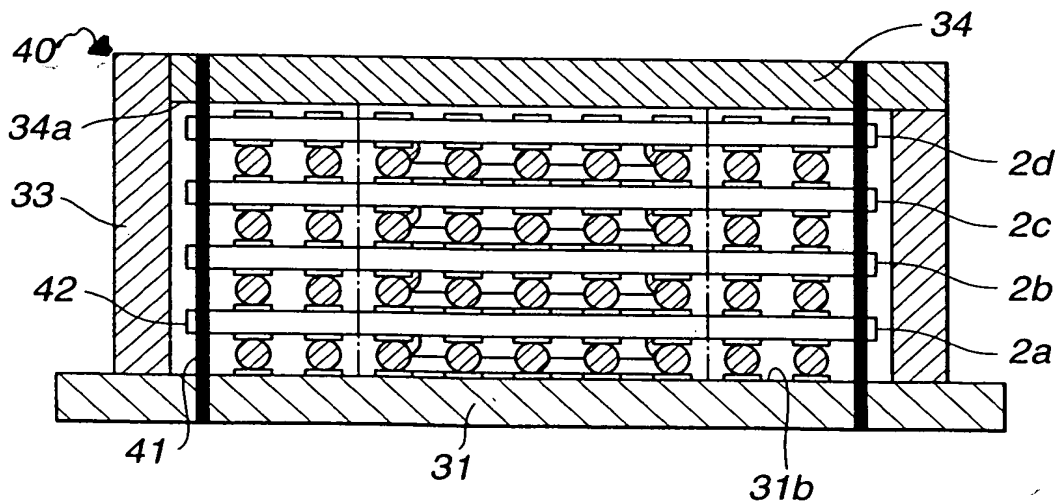
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**FIG. 5(a)**



**FIG. 5(b)**



**FIG. 6**